# Analysis and Design of a 5-GHz Low Noise Phase Quadrature VCO Using Varactor Diode

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***Abstract***

A quadrature oscillator using active superharmonic coupling is introduced. In this, work , we present a method to obtain quadrate VCO based on the differential VCO. The circuit is simulated in standard 0.18 μm CMOS. This CMOS quadrature VCO shows very good performance with an amplitude of the first harmonic is 4.152dBm for fundamental, phase noise -110.1dBc/Hz for fundamental and -115.5dBc/Hz at a 1MHz offset.

***Keywords***

*Quadrature Voltage Controlled Oscillator(QVCO); Superharmonic Coupling; Phase Noise*

## Introduction

The rapid growth of new generation wireless communication systems has developed considerable demand for designing single-chip radio receiver and transmitter devices in a fully integrated CMOS process with very tiny sizes due to better integration, lower cost and lower operational voltage. In order to increase integration level, all passive components should be integrated seamlessly in a single chip. Oscillators are fundamental components in wireless communications systems that can be used for several applications. Communication systems that use phase shift keying modulation frequently require a pair of LO signals that are in quadrature, or 90° out- of-phase. Quadrature VCO(voltage control oscillator) is one of the most important components in direct conversion transceivers.These VCOs are of a basic role in image-rejection techniques which are based on the appropriate phasing of the signals. Furthermore, they eliminate the immense and non-planar high-frequency filters. it also should be added that, some digital radio communication systems (e.g. GSM and DECT) in which complex digital modulation schemes are applied in order to reduce the signal bandwidth to the possible minimum level, need quadrature VCO (Abidi A., 1995). In all the applications mentioned above, departures from the quadrature phase or the existence of an amplitude imbalance between the two signals leads to a damaging effect on the performance of the whole system. There are a number of techniques which can be applied to produce quadrature signals.One straight-forward method is to use an RC-CR phase shift network with a standard oscillator to create a 90° phaseshift (Craninckx J.; Steyaert M.S.J., 1998). Since the phase shift is completely dependent on the values of the resistors and capacitors, any deviation in the fabricated values of these components will directly lead to a phase error. Resistors in particular have large tolerances in most CMOS processes, and therefore this method can lead to poor accuracy in the quadrature signals that are generated. Another approach to generate quadrature signals is to use a digital frequency divider that follows an oscillator running at twice the fundamental frequency (Rofougaran A.; Rael J.; Abidi A., 1996). The use of this technique at high frequencies is inherently limited since an oscillator operating at double the desired frequency is required. A third common technique is to force two VCOs to run in quadrate by using coupling transistors working at the fundamental frequency (Vancorenland P.; Steyaert M., 2001). This technique suffers from a trade-off between quadrature accuracy and phase noise due to the effects of the coupling.The fourth method is to use a active polyphase filters such as ring oscillator desins. For instance, in four-delay stage ring oscillators, taps at diametrically opposite points yield quadrature phases. (Liu Z.; Evans R., 2008). In this work active superharmonic coupling was used to design a 5.0 GHz quadrate oscillator in CMOS 0.18 μm technology .Our QVCO works base on the 180 degrees phase shift between the second harmonics of two Cross-Couple VCOs.

## Phase Noise in Oscillator

The analysis of phase noise in electrical oscillators has always been a subject of theoretical and practical expr-

iments. This is ofcourse not unwarranted, since phase noise in oscillators is still one of the main bottlenecks in today's transceiver systems. Electrical behavior of a differential oscillator is based on push-pull operation of two identical out phase oscillators with virtual ground. Tank voltage is sinusoid in inputs of transistors due to high Q factor of factor of paralleled resonant circuit and thus harmonic attenuation (damping) is provided. In this way, odd order current harmonics in tank neutralize each other. At the same time, idealized alternative operation condition with 180 degree conduction angle for each component (50% of working cycle) reduces odd harmonic level, thus it leads to half-cosine current pulses in component drain ends. Dc current and even harmonics flow in tracking current source transistor. As a result, phase noise performance of a differential oscillator can be determined with negative resistance during half circle of oscillations like determining performance of a LC single output tank oscillator. Sideband phase noise of oscillator unit has negative resistance which is written as Leeson equation with experimental analogy for heat-induced phase noise of a feedback oscillator and it is obtained as follows:

$$L(f_m) = \frac{kTF}{2P_L}\left(\frac{f_0}{Q_L f_m}\right)^2 \quad (1)$$

A pair of differential transistors with cross coupling provide negative resistance. This pair is connected to a LC tank. It is assumed that the output is buffered so that external load is separated from oscillator and variable capacitors are composed of a pair of pMOS varactor. In Eq. 1, PL represents wasted power in load resistance RL, QL is Q factor of resonant circuit, and F = Rn/RL is noise factor.

Now consider constituent elements of the real oscillator circuit separately. Considering losses in reactive elements of the resonant circuit, Q factor of a QL resonator can obtain inductor Q factor ($Q_{ind}$ = $R_{pL}/\omega L$) and capacitor Q factor ($Q_{cap}$ = $\omega CR_{pC}$) using following equation:

$$\frac{1}{Q_L} = \frac{1}{Q_{ind}} + \frac{1}{Q_{cap}}\frac{C}{C+C_P} \quad (2)$$

where Cp is sum of component output's capacitance, loading capacitance due to buffer stage and parasitic implementation capacitance.

## Designe Of a 5 GHz Quadrate VCO

A common method for implementing CMOS differential LC oscillators is using a cross-coupled pair for developing negative resistance in order to overcome losses in tank. The resistance related to cross-coupled pair is obtained by $-2/g_m$ where gm is mutual conductance of each BJT in cross-coupled pair. Thus, required negative resistance can be achieved for contrasting and neutralizing losses in tank by appropriate selection of size and biasing.The cross-coupled VCO is the most frequently used microwave VCO topology in CMOS technology. We can prepare a model of a LC VCO with the capacitor and inductor, parallel with a resistor to simulate the losses in the tank, and also a negative resistance to simulate the active device. in order to produce the negative resistance to compensate for the losses in the LC tank, employing a cross-coupled differential pair, as shown in Figure 1, would be a choice.

$g_m$ is the transconductance of each of the BJTs in the cross-coupled pair. Therefore, by choosing a proper device size and biasing, the value of negative resistance necessary to counteract, we are able to find the losses in the tank.

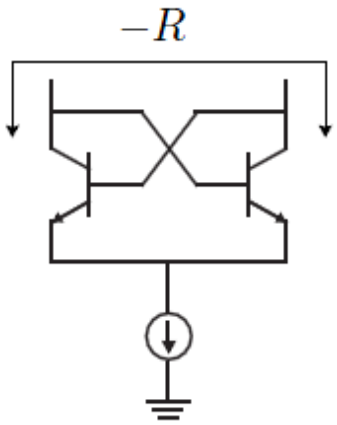


FIGURE 1. NEGATIVE RESISTANCE GENERATED FROM CROSS-COUPLED

BJT, R=2/ $g_m$

Figure2, illustrates a frequently employed LC VCO circuit using the cross coupled differential pair. A moderately low supply voltage is possible to be used for this implementation because there are only two levels of transistors.CMOS technology was applied to design fundamental C band VCO for the present experiment. The Diode varactor illustrated in Figure2 allows the tuning of frequency. DC blocking capacitors were used so that it is possible to bias transistors for optimal connection. Since every practical application of oscillators requires connecting its outlet to other circuits, buffer should be used so that it is guaranteed that loading does not disturb oscillations. Source tracking buffers should be used for four outlets so that

oscillator can be evaluated using equipments of 50 Ω input impedances. Resistors in particular have large tolerances in most CMOS processes, and therefore this method can lead to poor accuracy in the quadrature signals that are generated.

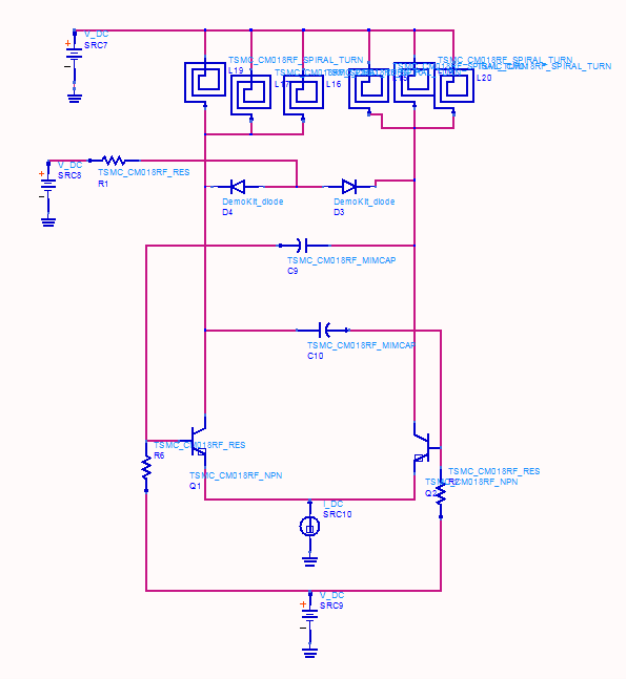

FIGURE 2. PROPOSED LOW NOISE CROSS-COUPLED BJT VCO

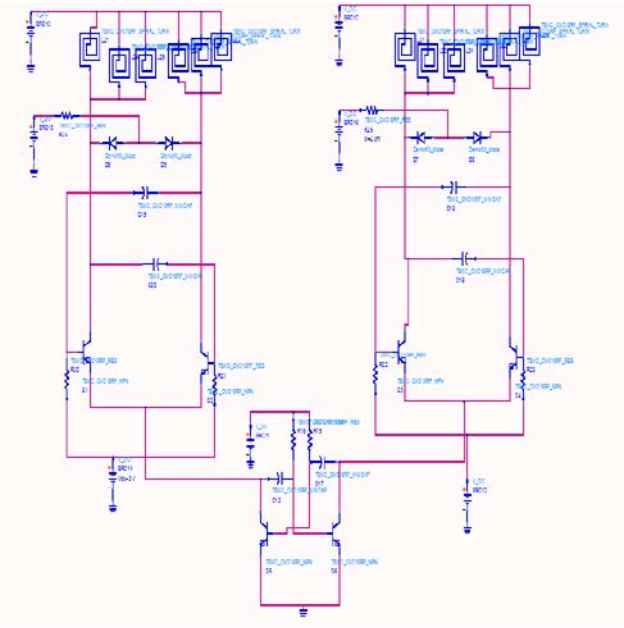

FIGURE 3. QUADRATURE OSCILLATOR CIRCUIT USING ACTIVE SUPERHARMONIC COUPLING

Another approach to generate quadrature signals is to use a digital frequency divider that follows an VCO running at twice the fundamental frequency (Maligeorgos J.P and Long J.R, 2000). The use of this technique at high frequencies is inherently limited since an VCO operating at double the desired frequency is required. A third common technique is to force two VCOs to run in quadrature by using coupling transistors working at the fundamental frequency (Rofougaran A, 1998)This technique suffers from a trade-off between quadrature accuracy and phase noise due to the effects of the coupling circuit on the oscillation frequency. To avoid this problem, a quadrature VCO can be realized using superharmonic coupling. By employing differential coupling at the common-mode nodes where the second harmonic is predominant, quadrature signals are generated at the fundamental frequency. To implement the coupling of the second harmonic with a 180° phase shift, an inverting on-chip transformer has been used (Meng C.; Chang Y.W.; Tseng S.C, 2006)-( Gierkink S, Levantino S, Frye R, Samori C, and Boccuzzi V, 2003). However, on-chip transformers consume a significant area on-chip and have a limited Q-factor, particularly in CMOS technology. The superharmonic coupling technique enforces an $180^0$ relationship between the even-ordered harmonics of two VCO circuits. While both passive and active superharmonic coupling circuits are possible. The performance of a quadrature VCO using the superharmonic coupling topology will be determined by the performance of the two individual dierential VCO as well as the coupling network. That enforces the anti-phase relationship between the second-order harmonics at the common-mode nodes. A very common way of implementing a CMOS differential LC VCO is to use a cross-coupled pair to generate the negative resistance required to overcome the losses in the tank. Therefore, with an appropriate device size and biasing, the negative resistance required to counteract the losses in the tank can be realized. The core quadrature VCO circuit investigated in this work is shown in Figure 3. It consists of two cross-coupled VCO connected through a cross coupled pair. It has been shown that by including cross-coupled inductor above the cross-coupled NPN transistors the phase noise of the VCO can be improved significantly due to the higher transconductance and faster switching speed of the complementary structure (Xueyang Geng Dai, F.F, 2010). The oscillation frequency for each VCO can be found from the familiar formula for the resonant frequency of an LC tank, where L is the value of the on-chip spiral inductor and C is the total capacitance at the tank nodes. The inductors used in this circuit

less than 1.3nH. The total capacitance including the lumped capacitor as well as the parasitic capacitance was 0.935pF to provide oscillation at 5GHz. The network used to enforce the $180^0$ phase difference in the second-order harmonics is a critical part of the quadrature VCO. It is this anti-phase relationship that creates the quadrature phase relationship at the fundamental frequency.In Figure 3 DC blocking capacitors were used so that transistors Q5-Q6 could be biased for optimal coupling. Since any practical use of an VCO involves connecting its output to other circuitry, buffers must be used to ensure that loading does not disrupt the oscillations. Source follower buffers were used for each of the four outputs so that the VCO can be measured using equipment with $50\,\Omega$ input impedances. The current sources shown in the buffer .

The $180^0$ and $270^0$ outputs were terminated on-chip with $50\,\Omega$ loads and the $0^0$ and $90^0$ were connected to CPW pads for on-chip probing.

## Simulation Results

### *Simulation Results for Cross-coupled VCO*

The amplitude of the first harmonic is 4.152dBm and the phase noise at a 1 MHz offset was -110.134dBc/Hz.

Figure 4 illustrates the phase noise graph. Figure 5 illustrates amplitude of the first harmonic and Figure 6 illustrates Time-domain VCO outputs.

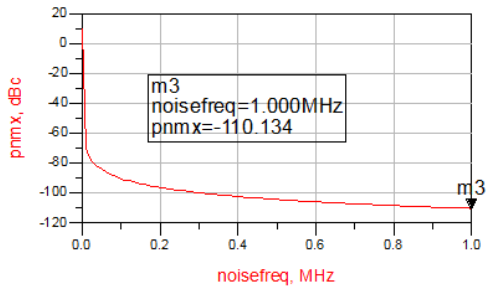


FIGURE 4. PHASE NOISE FOR CROSS-COUPLED VCO

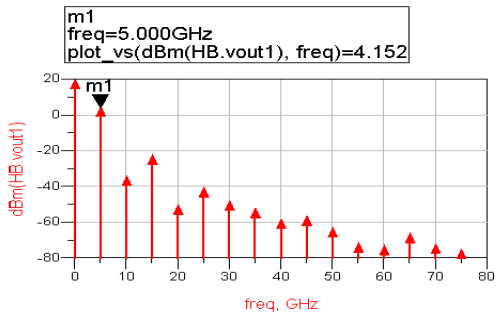


FIGURE 5. AMPLITUDE OF THE FIRST HARMONIC

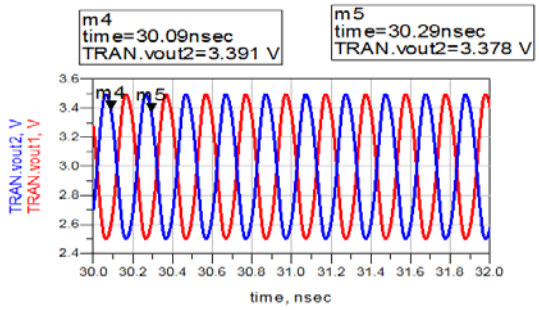


FIGURE 6. TIME-DOMAIN CROSS-COUPLED VCO

### *Simulation Results for QVCO*

In Quadrature VCO at subharmonic frequency (10GHz) the phase noise at a 1 MHz offset was -115.5dBc/Hz.Figure 7 shows spectrum of output. Figure 8 shows Graph of phase noise. And Figure 9 shows Time-domain VCO outputs. Table 1 shows result of compare with other VCO designs.

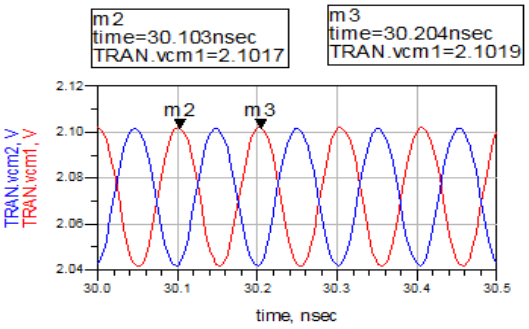


FIGURE 7. QVCO OUTPUTS IN VCM1 AND VCM2

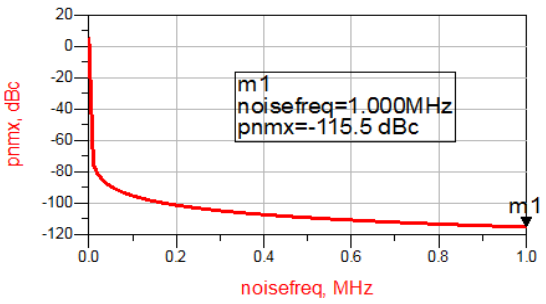


FIGURE 8. PHASE NOISE FOR QVCO

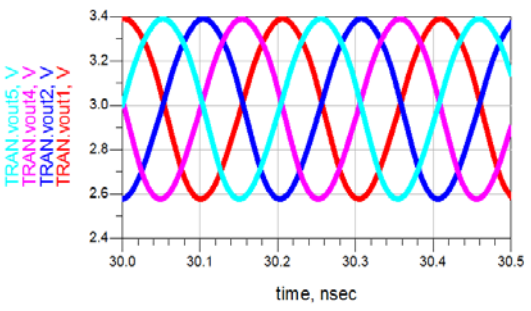

FIGURE 9. TIME-DOMAIN QVCO

TABLE 1. COMPARE WITH OTHER VCO DESIGNS

| Reference | $f_c$(GHz) | Phase noise(dBc/Hz) | Device |
|---|---|---|---|
| (Xueyang Geng Dai F.F, 2010) | 8.7 | -110 | SiGe BiCMOS |
| (Thanachayanont A, Krairiksh M, 2010) | 2.2 | -111 | CMOS0.35 μm |
| (Wu Y, Ismail M, and Olsson H, 2000) | 11.02 | -86.83 | CMOS RF |
| (Tang A, F.; Yuan F and Lawkrairiksh E, 2009) | 1.6 | -114.7 | CMOS 0.18 μm |
| This work | 10 | -115.5 | CMOS 0.18 μm |

## Conclusion

This paper represents a CMOS quadrature VCO which was designed at 5 GHz by applying superharmonic coupling. This technique focuses on coupling the second-order harmonics between two VCO and obliges an anti-phase connection, which, in turn, compels quadrature relationship at the fundamental. In order for this coupling with a $180^0$ phase shift to be implemented, a cross-coupled differential NPN pair was employed at the common-mode nodes. This CMOS quadrature VCO which employs an active superharmonic coupling demonstrates a very fine performance with an output power of 4.152dBm for fundamental, phase noise of -110.134dBc/Hz for fundamental and -115.5dBc/Hz at a 1MHz offset. It creates the $180^0$ phase shift in the second-order harmonics by using a cross-coupled differential pair.

## REFERENCES


Abidi, A.A.,"Direct-conversion radio transceivers for digital wmmunications ",*IEEE Journal of Solid-state Circuits*; Vol.30 Issue: 12, Dec. 1995, pp. 1399 -1410

Craninckx, J.; Steyaert, M.S.J. " A hlly integrated GaAs DCS-1800 frequency synthesizer", IEEE Journal of Solid-state Circuits,Vol.33,Issue:12,M.1998, pp.2054 -2065.

Rofougaran, A.; Rael, J.; Rofougaran, M.; Abidi, " A 900 MHz CMOS LC-oscillator with quadrature outputs," Solid- State Circuits Conference. 42nd ISSCC, IEEE International ,1996, pp. 392-393

Vancorenland, P.; Steyaert, M."A 1.57 GHz Mly integated very low phase noise quadrature VCO, " VLSI Circuits, Digest of Technical Papers. 2001 Symposium on, pp. 111-114,201

Liu.Z, E. Ska_das, and Evans.R, "A 60 GHz VCO with 6 GHz Tuning Range in 130 nm Bulk CMOS, " IEEE J. Solid-state Circuits., vol. 1, April 2008, pp. 209-211

Maligeorgos J.P and Long J.R, "A low-voltage 5.1-5.8 GHz imagereject receiver with wide dynamic range," IEEE J. Solid-state Circuits, vol.35, Dec. 2000. pp.1917-1926

Rofougaran.A et al., "A single-chip "A-voltage 5.1-5.8GHz imagereject900-MHz spread-spectrum wireless transceiver in 1-$\mu m$ m CMOS-Part I: Architecture and transmitted design," IEEE Journal of Solid-State Circuits, vol. 33, Apr. 1998, pp. 515-534

Meng.C, Chang.Y.W, S.C,Tseng,"4.9-GHz low-phase-noise transformer-based superharmonic coupled GaInP/GaAs HBT QVCO,"IEEE Microwave and Wireless Component Letters, vol1.16, no.6, June2006,pp.339-341.

Cabanillas. J, Dussopt. L, Lopez-Villegas. J, and Rebeiz. G, "A 900 MHz low phase noise CMOS quadrature oscillator," IEEE Radio Frequency Integrated Circuits Symposium, 2002

Gierkink. S, Levantino. S, Frye. R, Samori. C, and Boccuzzi. V,"A low-phase-noise 5-GHz GaAs quadrature VCO using superharmonic coupling," IEEE Journal of Solid-State Circuits, vol.38, no.7, July 2003, pp. 1148-1154.

Xueyang Geng Dai, F.F, "An x-band transformer-coupled varactor-less quadrature current-controlled oscillator in 0.18 $\mu m$ SIGE BICMOS," IEEE Journal of Solid-State Circuits, vol. 45, no. 9, August 2010, pp. 1669 - 1677.

Apinut Thanachayanont, Monai Krairiksh"Implementation of an rf CMOS quadrature lc voltage-controlled oscillator based on the switched tail transistor topology" world scint, Journal of circuit system and computer, vol. 20, no. 7, January 2010,pp. 1280 -1285.

Wu. Y, Ismail. M, and Olsson. H, An 8.7-13.8 GHz Transformer-coupled Varactor-less Quadrature vco," in Proc. IEEE Int. Symp. Circuit and System (ISCAS), Geneva, Switzerland May 2000, pp. 149–152.

Tang. A.F, Yuan. F and Lawkrairiksh. E "CMOS active transformers and their applications in voltage-controlled quadrature oscillators," Analog Integrated Circuits and Signal Processing, vol. 62, no. 1, Jun 2009, pp. 83-90.